

### Quadruple 2-Input Exclusive OR Gate IC in bare die form

Rev 1.0 14/05/25

### Description

The 54ACT86 exclusive OR gate (XOR) is fabricated using an advanced CMOS process which combines the high speed performance of LSTTL with CMOS low power consumption. This device contains four independent gates and performs the Boolean functions  $Y = A \oplus B \text{ or } Y = \overline{A}B + A\overline{B}. \text{ The device is characterized over the full military temperature range. Device inputs directly accept LSTTL or CMOS. All inputs are protected against ESD and excess voltage transients.$ 

### Ordering Information

The following part suffixes apply:

- No suffix MIL-STD-883 /2010B Visual Inspection
- "H" MIL-STD-883 /2010B Visual Inspection+ MIL-PRF-38534 Class H LAT
- "K" MIL-STD-883 /2010A Visual Inspection (Space)
   + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

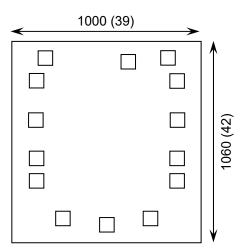
# Supply Formats:

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 280µm(11 Mils) On request
- Assembled into Ceramic Package On request

### Features:

- Inputs directly accept TTL
- Outputs directly interface CMOS, NMOS and TTL
- Outputs Source/Sink 24 mA
- Low Input Current: 1µA
- Functionally compatible with bipolar 54LS86
- Lower power alternative to bipolar logic
- Full Military Temperature Range

## Die Dimensions in µm (mils)



# **Mechanical Specification**

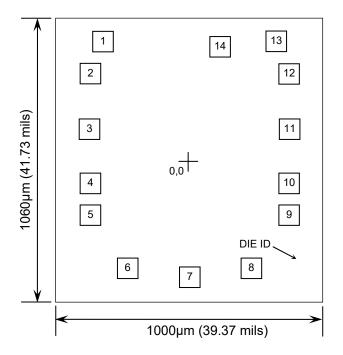
Die Size (Unsawn)	1000 x 1060 39 x 42	µm mils
Minimum Bond Pad Size	70 x 70 2.76 x 2.76	μm mils
Die Thickness	280 (±20) 11.02 (±0.79)	μm mils
Top Metal Composition	Al 1%Si 2μn	n
Back Metal Composition	N/A – Bare S	Si





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# Pad Layout and Functions



DAD EI	FUNCTION	COORDIN	ATES (µm)				
PAD	FUNCTION	X	Y				
1	A1	-296.8	407.5				
2	B1	-342.1	297.5				
3	Y1	-344.7	107				
4	A2	-342.1	-80				
5	B2	-342.1	-190				
6	Y2	-213.3	-372.7				
7	GND	0	-404.2				
8	Y3	213.3	-372.7				
9	A3	342.2	-190				
10	В3	342.2	-80				
11	Y4	344.8	107				
12	A4	342.2	297.5				
13	B4	296.9	407.5				
14	V <sub>CC</sub>	105.1	391.4				
CONNECT CHIP BACK TO V <sub>CC</sub> OR FLOAT							

# Logic Diagram

A1 
$$\frac{1}{2}$$
  $\frac{3}{2}$  Y1

A2  $\frac{4}{5}$   $\frac{6}{5}$  Y2

Y = A  $\oplus$  B

=  $\overline{A}B + A\overline{B}$ 

A3  $\frac{9}{10}$   $\frac{8}{10}$  Y3

A4  $\frac{12}{13}$   $\frac{11}{10}$  Y4

# **Function Table**

INP	UTS	OUTPUT				
Α	В	Υ				
L	L	L				
L	H	Н				
Н	L	Н				
Н	Н	L				
H = H	H = High level (steady state)					

H = High level (steady state) L = Low level (steady state)



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# Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V <sub>CC</sub>	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V <sub>IN</sub>	-0.5 to V <sub>CC</sub> +0.5	V
DC Output Voltage (Referenced to GND)	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V
DC Input Current	I <sub>IN</sub>	±20	mA
DC Output Current, per pad	l <sub>out</sub>	±50	mA
DC Supply Current, V <sub>CC</sub> or GND, per pad	I <sub>cc</sub>	±50	mA
Power Dissipation in Still Air <sup>2</sup>	P <sub>D</sub>	750	mW
Storage Temperature Range	T <sub>STG</sub>	-65 to 150	°C

<sup>1.</sup> Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

# Recommended Operating Conditions<sup>3</sup> (Voltages Referenced to GND)

1 5		, ,		,
PARAMETER	SYMBOL	MIN	MAX	UNITS
DC Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
DC Input or Output Voltage	$V_{IN}$ , $V_{OUT}$	0	V <sub>CC</sub>	V
Operating Temperature Range	T <sub>J</sub>	-55	+125	°C
Output current - High	I <sub>OH</sub>	-	-24	mA
Output current - Low	I <sub>OL</sub>	-	24	mA
Input Rise or Fall rate V <sub>CC</sub> = 4.5V	Λ+/Λ\ <i>/</i>	0	10	ns/V
$(V_{IN} \text{ from 0.8V to 2V})$ $V_{CC} = 5.5V$	Δt/ΔV	0	8	TIS/V

<sup>3.</sup> This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range GND  $\leq$  ( $V_{IN}$  or  $V_{OUT}$ )  $\leq$   $V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

### DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	CVMDOL	V	CONDITIONS		LIMI	LINUTO	
	STIMBUL	SYMBOL V <sub>cc</sub> COM	CONDITIONS	25°C	85°C	FULL RANGE⁴	UNITS
Minimum High-Level	W	4.5V	V <sub>OUT</sub> = 0.1V	2	2	2	V
Input Voltage	V <sub>IH</sub>	5.5V	or V <sub>CC</sub> -0.1V	2	2	2	V
Maximum Low-Level	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	4.5V	$V_{OUT} = 0.1V$	0.8	8.0	0.8	V
Input Voltage	V <sub>IL</sub>	5.5V	or V <sub>CC</sub> -0.1V	0.8	8.0	0.8	V
Minimum Low-Level Output Voltage		4.5V	I <sub>OUT</sub> = 50μA	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
	4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^{5}$	0.36	0.44	0.50	V	
	V <sub>OL</sub> 5.5V	5.5V	$I_{OL} = 24mA$	0.36	0.44	0.50	V
		4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^{5,6}$	-	-	1.65	V
		5.5V	$I_{OL} = 50 \text{mA}$	-	-	1.65	\ \ \

<sup>4. -55°</sup>C ≤  $T_J$  ≤ +125°C 5. All outputs loaded; thresholds on input associated with output under test. 6. Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75 $\Omega$  transmission-line drive capability at 125°C





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# DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	W	V <sub>cc</sub> CONDITIONS	LIMITS			UNITS
	STIVIDOL	STIVIBUL V <sub>CC</sub>		25°C	85°C	FULL RANGE⁴	UNITS
		4.5V	I - 50uA	4.4	4.4	4.4	V
Minimum High-Level	W	5.5V	I <sub>OUT</sub> = 50μA	5.4	5.4	5.4	V
Output Voltage	V <sub>OH</sub>	4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^5$	3.86	3.76	3.7	V
		5.5V	$I_{OH} = -24mA$	4.86	4.76	4.7	V
Maximum Input Leakage Current	I <sub>IN</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0	μA
Additional Maximum I <sub>CC</sub> / Input	ΔI <sub>CCT</sub>	5.5V	$V_{IN} = V_{CC} - 2.1V$	0.6	1.5	1.6	mA
Minimum Dynamic	I <sub>OLD</sub>	5.5V	V <sub>OLD</sub> = 1.65V Max	-	75	50	mA
Output Current <sup>7</sup>	I <sub>OHD</sub>	5.5V	V <sub>OHD</sub> = 3.85V Min	-	-75	-50	IIIA
Maximum Quiescent Supply Leakage Current	I <sub>CC</sub>	5.5V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	4	40	80	μА

<sup>7.</sup> Maximum test duration 2ms, one output loaded at a time.

# AC Electrical Characteristics<sup>8</sup> V<sub>cc</sub> = 5.0V ±0.5V

DADAMETED	PARAMETER SYMBOL V <sub>cc</sub>	V	V CONDITIONS	LIMITS			UNITS
PARAMETER		V <sub>cc</sub> CONDITIONS	25°C	85°C	FULL RANGE⁴	UNITS	
Maximum Propagation Delay	t <sub>PLH</sub>	5.0V	C <sub>L</sub> = 50pF,	9.5	10	14.6	
Input A or B to Output Y (Figure 1)	·	5.0V	Input tr = tf =3.0ns	9.5	10.5	14.6	ns
Maximum Input	C <sub>IN</sub>	5.0V	T <sub>J</sub> = 25°C		TYPIC	AL	pF
Capacitance	JIN C	3.0 V	15 20 0		4.5		рі
Power Dissipation Capacitance	C <sub>PD</sub>	5.0V	$T_J = 25$ °C, $C_L = 50$ pF		35		pF

<sup>8.</sup> Not production tested in die form, characterized by chip design.





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# **Switching Waveform**

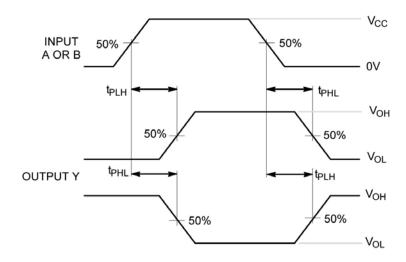


Figure 1 - Propagation Delay

# Test Circuit 1kΩ R<sub>pd</sub> OUTPUT TEST POINT C<sub>L</sub>\*

\* Includes all probe and jig capacitance

Figure 2

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